

**IN THE ABSTRACT:**

Please replace the previous abstract with the following new abstract:

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C<sup>1</sup> A high-voltage MOS transistor wherein a dopant concentration of a source offset region is set lower than a dopant concentration of a drain offset region whereby a resistance value of the source region is set independently of a resistance value of the drain region in such a manner as to maintain a high sustaining breakdown voltage of the high-voltage MOS transistor, which is based on a voltage of the source offset region and a voltage of a substrate region directly under a gate insulating film during operation of the high-voltage MOS transistor.

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